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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,204	12/05/2001	Geeng-Chuan Chern	2102397-991220	2140

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EXAMINER	
GREENE, PERSHELLE L	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/008,204	CHERN ET AL.
	Examiner	Art Unit
	Pershelle Greene	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,28 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 28-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/008204
Attorney's Docket #: 2102397-991220

Filing Date: 12/05/2001

Applicant: Chern et al.
Examiner: Pershelle Greene

DETAILED ACTION

Please note that applicant's arguments are not found to be persuasive. The previous rejection still stands and is restated below. The limitation that the insulating layer is initially formed as a continuous layer of material, is not relevant to do with the final device that is being claimed. The examiner is only concerned with the final device that is being claimed. Also note that since there are two insulating layers formed one on top of the other, therefor the two layers can be used to represent the one insulating layer.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4-8, and 28 are being rejected under 35 U.S.C. 103(a) as being anticipated by Hoang (U. S. Patent # 6,420,753), in view of Chiu (U.S. Patent # 5,021,848).

As to claim 1, Hoang discloses electrically selectable and alterable memory cells having all of the claimed subject matter:

A. "a substrate ... and a peripheral area" is met by the substrate 200 of semiconductor material that includes a memory area (right side of 208) and a peripheral area (208 and everything to the left) shown in figure 6;
B. "an electrically ... from the substrate" is met by the electrically conductive floating gate 204 disposed over and insulated from the substrate 200 shown in figure 6;
C. "an electrically ... to the floating gate" is met by the electrically conductive control gate 210 disposed adjacent to the floating gate 204 shown in figure 6;
D. "an insulating layer ... tunneling of charges therethrough" is met by the insulating layer 206 formed in the memory area and peripheral areas that includes a first portion that is disposed between the control gate 210 and the floating gate 204 with a thickness permitting Fowler-Nordheim tunneling of charges. Refer to figure 6 and column 2 lines 4-15;
E. "an electrically ... from the substrate" is met by the electrically conductive select gate 208, which can be made of polysilicon, disposed over and insulated from the substrate 200. Refer to figure 6 and column 13 lines 33-45;
F. "a second portion of the insulating layer ... of the insulating layer" is met by the second potion of the insulating layer (206 202) being disposed between the poly

gate 208 and the substrate 200 and having a thickness that is greater than that of the first portion of the insulating layer 206 shown in figure 6;

Hoang fails to explicitly show the insulating layer being initially formed as a continuous layer of material. However the fact that the insulating layer is not initially formed as a continuous layer does not change the operation of the device nor does it change the final structure of the device that is being claimed.

Chiu is cited for showing an electrically-erasable and electrically-programmable memory storage devices with self-aligned tunnel dielectric area. Specifically, Chiu is cited for showing a continuous insulating layer 21 having a first portion disposed between the control gate and the floating gate and a second portion disposed between the poly gate and the substrate and having a thickness that is greater than that of the first portion of the insulating layer.

It would have been obvious to one of ordinary skill in the art to use the continuous insulating layer of Chiu with the device of Hoang for the purpose of reducing manufacturing cost and manufacturing materials.

As to claim 2, Hoang shows in figure 6 a source region 214 and a drain region 214 formed in the substrate having a channel region in between. The floating gate 204 is disposed over and insulated from a portion of the channel region.

As to claims 4-6, Hoang shows in figure 6 the control gate 210 having a first portion that is disposed over the floating gate 204. The first portion of the control gate 210 is also disposed over a portion of the channel region. The second portion of the control gate 210 is disposed over the floating gate 204.

As to claims 7-8, Hoang shows the device has an insulating layer with a second portion formed directly on the peripheral area of the substrate. The poly gate 208 is formed directly on the second portion of the insulating layer. The first portion of the insulating layer extends between the substrate 200 and the control gate 210.

3. Claim 3 is being rejected under 35 U.S.C. 103(a) as being unpatentable over Hoang (U. S. Patent # 6,420,753), in view of Chiu (U.S. Patent # 5,021,848), and further in view of Furuhata et al. (U. S. Patent # 6,429,073).

As to claim 3, claim 3 is being rejected for the same reasons set forth in regard to claim 1. In addition, Furuhata et al. discloses, in figure 1, a second source and drain region formed in the substrate, with a second channel region in between. The poly gate 30 is disposed over and insulated from at least a portion of the second channel region.

4. Claims 9-14 and 29 are being rejected under 35 U.S.C. 103(a) as being unpatentable over Hoang (U. S. Patent # 6,420,753), in view of Chiu (U.S. Patent # 5,021,848), and further in view of Furuhata et al. (U. S. Patent # 6,429,073).

In claims 9-14 and 29, Hoang shows, in figure 6, a substrate of semiconductor material having a memory area and a peripheral area. There is a memory cell in the memory area that includes a first source region 214 and a first drain region 214 formed in the substrate having a channel region in between. There is an electrically conductive floating gate 204 that is disposed over and insulated from at least a portion of the first channel region. An electrically conductive control gate 210 is disposed adjacent to the floating gate 204. An insulating layer (206 202) is formed in the memory and peripheral area. The insulating layer has a first portion that is disposed between the control gate 210 and the floating gate 204 with a thickness permitting

Fowler-Nordheim tunneling of charges. Hoang fails to explicitly show a second source and drain region and the insulating layer being initially formed as a continuous layer of material. However the fact that the insulating layer is not initially formed as a continuous layer does not change the operation of the device nor does it change the final structure of the device that is being claimed.

Chiu is cited for showing an electrically-erasable and electrically-programmable memory storage devices with self-aligned tunnel dielectric area. Specifically, Chiu is cited for showing a continuous insulating layer having a first portion disposed between the control gate and the floating gate and a second portion disposed between the poly gate and the substrate and having a thickness that is greater than that of the first portion of the insulating layer.

It would have been obvious to one of ordinary skill in the art to use the continuous insulating layer of Chiu with the device of Hoang for the purpose of reducing manufacturing cost and manufacturing materials.

As to claims 10-12, Hoang shows in figure 6 the control gate 210 having a first portion that is disposed over the floating gate 204. The first portion of the control gate 210 is also disposed over a portion of the channel region. The second portion of the control gate 210 is disposed over the floating gate 204.

As to claims 13-14, Hoang shows the device has an insulating layer with a second portion formed directly on the peripheral area of the substrate. The poly gate 208 is formed directly on the second portion of the insulating layer. The first portion of the insulating layer extends between the substrate 200 and the control gate 210.

Furuhata et al. is cited for showing a method for manufacturing semiconductor devices having a non-volatile memory transistor. Specifically Furuhata discloses, referring to figure 1, a second source 16, drain 14 and channel region. The source 16, drain 14, and channel regions are formed in the substrate 10 with a channel region in between. The electrically conductive poly gate 30 is disposed over and insulated from at least a portion of the second channel region.

It would have been obvious to one of ordinary skill in the art to add the second source, drain, and channel region of Furuhata et al. to the device of Hoang for the purpose of reducing the potential of a noise problem and for better isolation.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pershelle Greene whose telephone number is 571-272-1917. The examiner can normally be reached on M-F 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

PLG
April 30, 2004

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800